Sigma-delta convertor for measurement technology

White Paper

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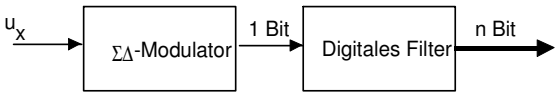
Recently, we have often heard of sigma-delta (ΣΔ) - converters being used in various test and measurement applications. In fact, in many imc Meßsysteme systems and devices (imc CRONOS*compact*, imc CANSAS, ...) these converters come as standard hardware. How does such a converter function, why is its importance increasing so rapidly and what are the benefits for the engineers and technicians? The purpose of this white paper is to address and provide answers and explanations to these questions.

The sigma-delta converter has shown to prevail in the audio technology applications and is currently penetrating deeper into the field of test and measurement. Especially for intelligent measurement systems, this conversion method is the most favored method. With it, high resolution and excellent signal-to-noise ratios (SNR = signal to noise ratio) can be achieved. The main advantage from the very beginning with these convertors in measurement devices is the anti-aliasing filter (see White Paper: "Choosing the correct sampling rate"). They are particularly simple and inexpensive, so that each measurement channel can be equipped with one. Because of the low prices of these components, measurement device architecture that doesn't come pre-equipped with an analog multi-plexer is becoming more and more rare.

The following figure shows a conversion from a 1-bit ΣΔ-modulator and a digital high-order filter. The modulator operates at a high, constant switching frequency (oversampling). The output rate of n bits after the digital filter is lowered according to the desired measuring rate (Decimation).

a) Block diagram



b) ΣΔ-modulator

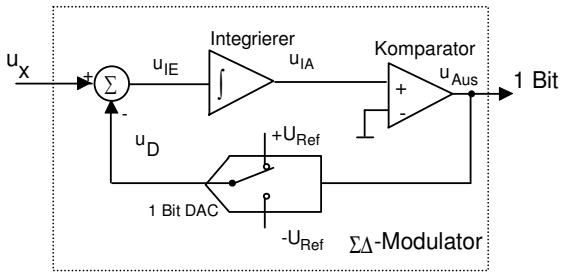


Figure 1: *ΣΔ-convertor*

The basic principle of the sigma-delta modulator is a loop consisting of integrator and comparator downstream. Because the comparator can only read the logical values of "1" and "0", and, consequently, the average difference between the 1 bit DAC signal and U_D and the input signal U_X must be exactly "0" (or else the integrator runs away), the mean value of the DAC signal must equal the input signal. Since the output signal is digital in nature, a 1 bit DAC must consequently change this signal back to an analog signal. The input voltage range for U_X results from $-U_{Ref} \leq U_X \leq U_{Ref}$. The mean value (equivalent to U_X) can be recovered through the digital low-pass filtering of the comparator signal.

As will be shown later, up to half of the sampling frequency results in a reduced noise power. As is additionally shown in the above figure, the control loop causes a shift of the noise spectrum at high frequencies (noise-shaping). This will also be shown in the following.

The 1 bit ADC is followed downstream by a low-pass digital filter. This results, on the one hand, in the filtering of the noise in the frequency range of interest, and on the other hand, a reduction of the sampling frequency can take place (decimation). With these convertors, resolutions between 16 and 24 bits are possible to achieve.

Quantization noise

First, some concepts should be clarified that are necessary for the understanding of the converter. This includes the concept of quantization noise. The quantization noise U_{Noise} is understood here as the difference between the voltage staircase and an ideal straight line. The higher the resolution of the converter is, the smaller the steps will be, and consequently, the quantization noise.

For a sinusoidal input signal with the peak value U_P it is true for the RMS:

$$U_{Signal} = u_p / \sqrt{2}$$

This expression, considering that 1LSB = 2 U_P /2^n is true, can be stated as such:

$$U_{Signal} = 1LSB\, 2^{n-1}/\sqrt{2}$$

The RMS value of the quantization noise corresponds to the following diagram:

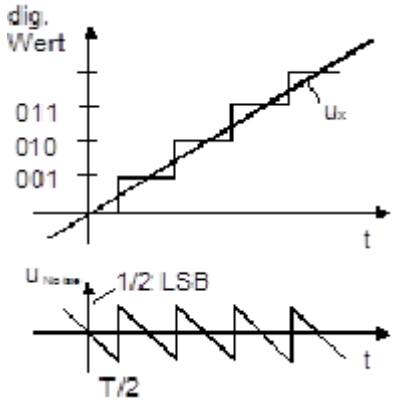


Figure 2: *RMS value of the quantization noise*

In general, it holds true that for the RMS value of the signal U_{Noise}:

$$U_{Noise} = \sqrt{\frac{1}{T}\int_T u_{Noise}^2 dt}$$

$$U_{Noise} = \sqrt{\frac{1}{T}\int_{-T/2}^{T/2} u^2_{Noise} dt} = 1LSB/\sqrt{12}$$

Thus, the signal-to-noise ratio (SNR) can be stated as such:

$$SNR = U_{Signal}/U_{Noise} = 2^n \frac{\sqrt{3}}{\sqrt{2}}$$

Expressing this ratio in dB:

$$SNR_{dB} = 20\log 2^n \sqrt{1{,}5} = 20\,(n\log 2 + \log 1{,}225)$$

it follows:

$$SNR_{dB} = 6{,}02\,n + 1{,}76$$

According to this equation, the SNR is for a 1-bit ADC results in only 7.78 dB. But for a 16 bit ADC, 98 dB must be achieved. This can be achieved with oversampling and noise shaping. It should be noted that the SNR_{dB} of the noise to the sampling frequency f_T:

$$SNR_{dB} = SNR\big|_{f_T}$$

Oversampling

According to the sampling theorem, it must be that in the measurement signal U_X may contain only relevant frequency components to f_T /2. If the highest relevant frequency of U_X is characterized as f_m, then the minimum holds true:

$$f_T = 2f_m$$

If the measurement signal U_X is oversampled (over-sampling) by a factor k (usually 32, 64), so that the measurement noise is distributed over a wide frequency range, it then results in a k-times oversampling:

$$f_T = k \cdot 2f_m$$

From the RMS noise voltage:

$$U_{Noise} = 1LSB/\sqrt{12}$$

results in the noise power:

$$P_{Noise} \sim (1LSB)^2/12$$

Since the noise extends over the frequency range from $-f_T/2$ to $f_T/2$, the result for the noise power density is then:

$$p_{Noise} \sim (1\,LSB)^2 / (12\,f_T)$$

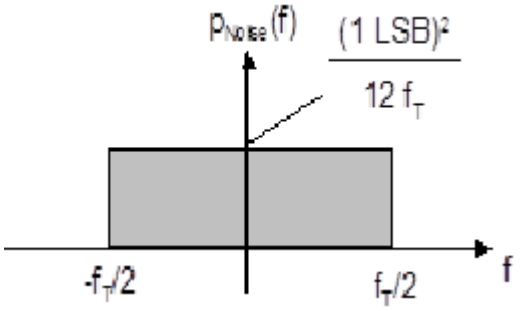


Figure 3: *Noise power density from oversampling*

If the sampling frequency f_T increases by a factor of k, then the noise power density must decrease by the same noise power by a factor of k.

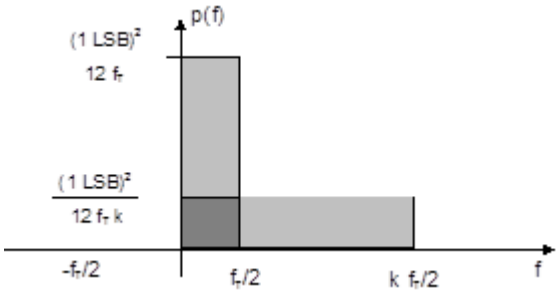


Figure 4: *Reduced noise power density by a factor of k*

This is the noise voltage in the frequency range of interest from 0 to $+f_T/2$ with the sampling frequency f_T:

$$U_{Noise}\Big|_{f_T} = \frac{1\,LSB}{\sqrt{12}}$$

and with the sampling frequency k f_T:

$$U_{Noise}\Big|_{kf_T} = \frac{1\,LSB}{\sqrt{12k}} = \frac{1\,LSB}{\sqrt{12}}\frac{1}{\sqrt{k}} = U_{Noise}\Big|_{f_T}\frac{1}{\sqrt{k}}$$

This means that through an oversampling of k times, the noise voltage is thus reduced by a factor of k times.

The signal-to-noise ratio results in taking into account the oversampling of k times.

$$SNR\Big|_{kf_T} = 20\log\left(\frac{U_{Signal}}{U_{Noise}\Big|_{kf_T}}\right) = 20\log\left(\frac{U_{Signal}}{U_{Noise}\Big|_{f_T}}\sqrt{k}\right)$$

$$SNR\Big|_{kf_T} = SNR\Big|_{f_T} + 10\log(k)\,\text{in dB}$$

This means that for a 1-bit converter with 64-times oversampling , an SNR is obtained of only 7,78dB + 18,06dB = 25,84dB. What is still completely inadequate is that for a 16-bit system at least 98dB must be achieved. Each doubling of the sampling frequency only results in an increase in the SNR by 3 dB.

A huge advantage of oversampling, however, is the fact that the anti-aliasing filter can easily be omitted (1st or 2nd order). This is because the sampling rate of the ADCs is very high and thus, no great challenges are placed on the steepness of the filter to avoid aliasing effects. Moreover, the oversampling frequency kf_t is kept constant, whereby the anti-aliasing filter does not have to be switchable. This represents a considerable cost reduction compared with conventional AD converters.

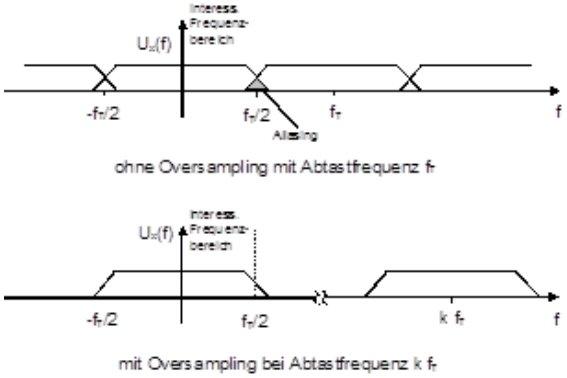


Figure 5: *Avoidance of aliasing effects due to oversampling*

Noise shaping

As will be shown in the following figure, the 1 bit modulator with the sampling frequency synchronized with the working comparator can be considered as a noise source U_{Noise} with the 1 bit noise. The downstream comparator of the 1-bit ADC just switches between the thresholds U_{Ref} and $-U_{Ref}$ and can therefore only be regarded as a level adjustment of the comparator

output signal. Thus, the modulator can be described by the following block diagram in which the noise spectrum can be moved.

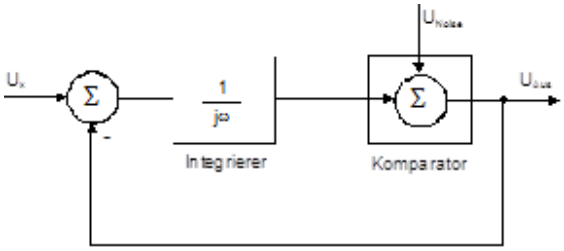


Figure 6: *Block diagram of a modulator*

The output signal U_{Aus} is given with the equation:

$$U_{Aus} = U_{Noise} + \frac{1}{j\omega}(U_x - U_{Aus})$$

In accordance with U_{Aus}, the results can be separated into:

$$U_{Aus} = \underbrace{\frac{U_{Noise}}{1+\frac{1}{j\omega}}}_{\text{Hochpass}} + \underbrace{\frac{U_x}{1+j\omega}}_{\text{Tiefpass}}$$

As can be seen from this equation, one obtains a low-pass filtered measured voltage U_X and a high-pass noise voltage U_{Noise}. As the following figure shows, only a small part of the noise will remain in the frequency range of interest due to the high pass.

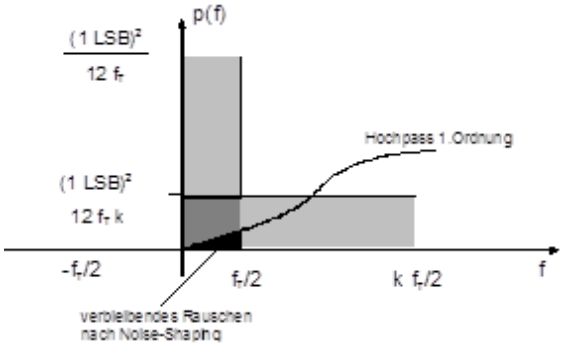


Figure 7: *Noise after noise shaping*

From these results, very high SNR values arise, so that one can achieve after the digital filter from bit numbers n between 16 to 24. In practice, sigma-delta modulators of higher order are used, so that the corresponding high-pass is also higher order and the noise is further reduced up to half of the sampling frequency.

After all the advantages that this conversion technology can have, of course you may wonder where the weaknesses of this AD converter are. A disadvantage may be that it takes a relatively long time (about 100 ... 200µs) until a value at the output of the converter (digital filter) is available. If you have multiple measurement channels that are delayed in the same way, for measurement purposes this doesn't necessarily represent a disadvantage, since all channels are delayed in this manner. If one wants to look at all the open- and closed-loop control tasks as a whole, then this delay is considered very fast for certain applications. Overall, however, the benefits of the converter with high resolution at relatively high sampling rates and the very simple anti-aliasing filter outweigh the disadvantages by far.

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